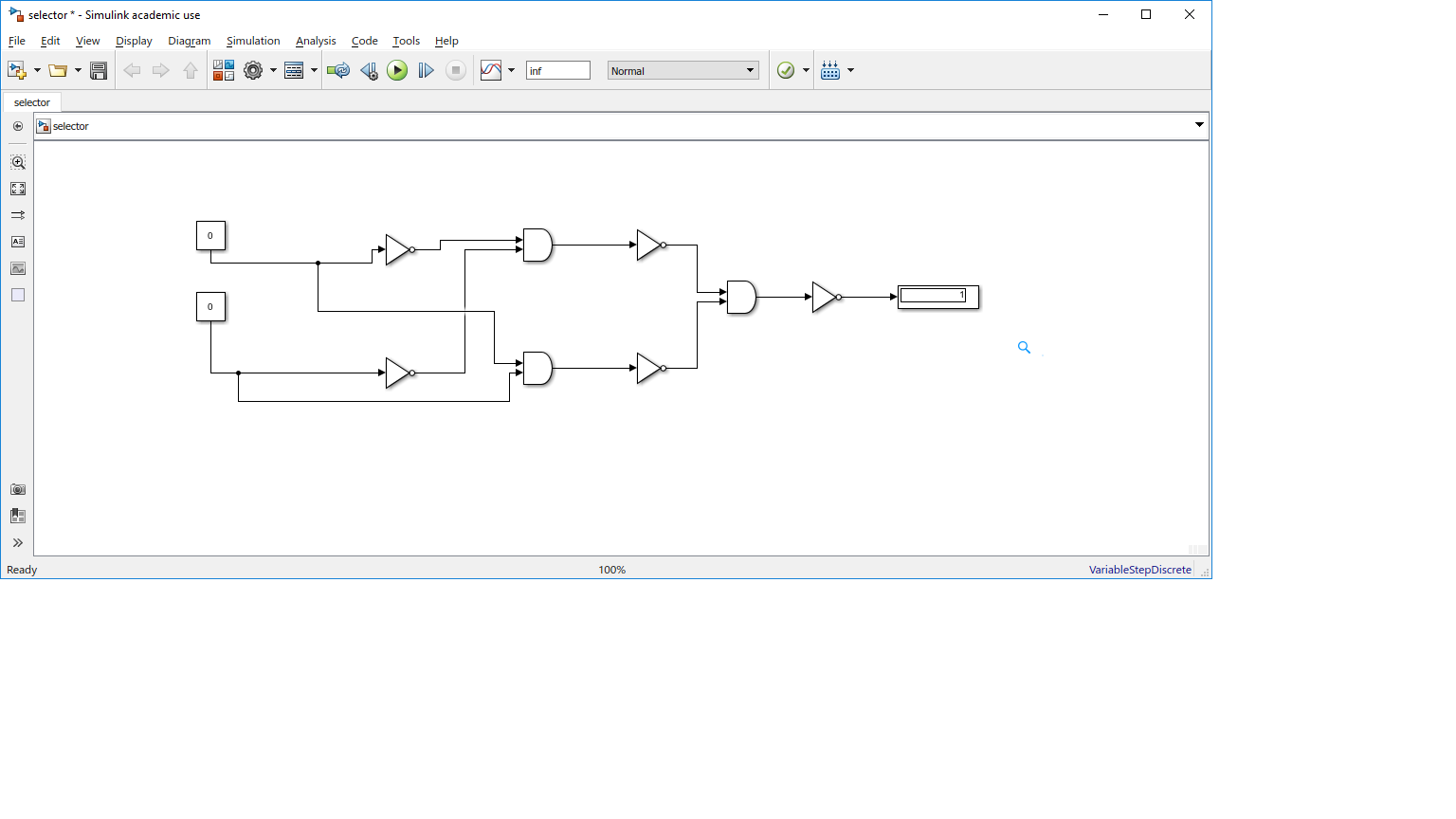
Introduction to Computer Systems 2018

Assignment 1

ID: 181509



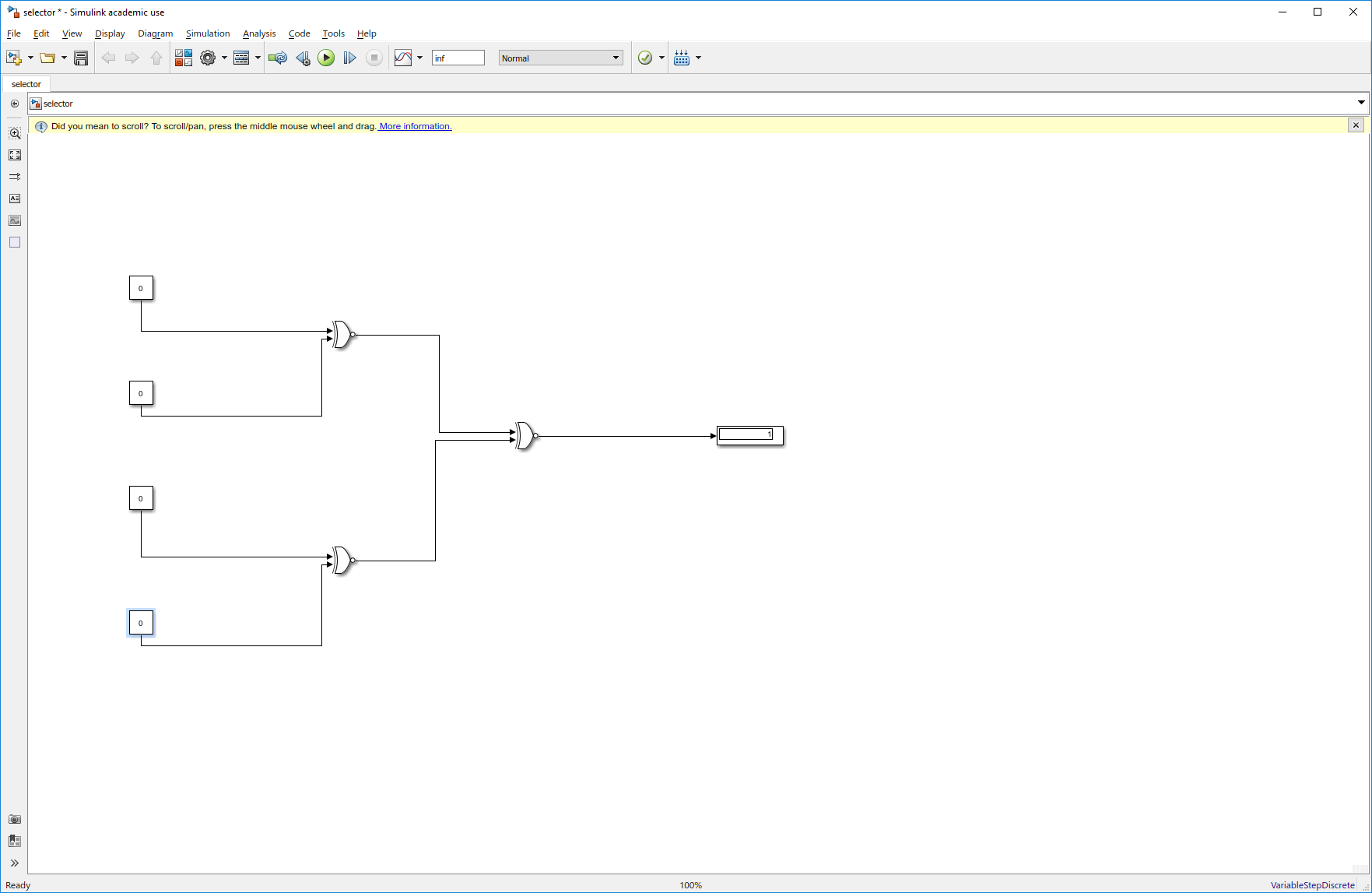
I tried using 2 inputs with 3 AND gates. Then I manipulated the circuit by using NOT gates in order to get the desired truth table.

Each input is used 2 AND gates; where one AND gate takes the input as it is and the other takes the input after it is processed through a NOT gate. Afterwards, each AND gate input is being inverted by NOT gates and taken by another AND gate. Finally, to get the desired truth table, the result of the final AND gate is inverted by another NOT gate and given as an output.

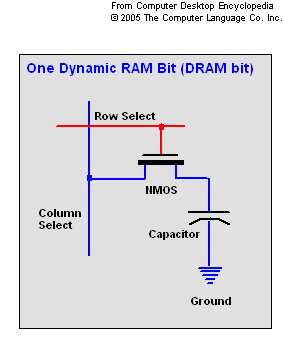
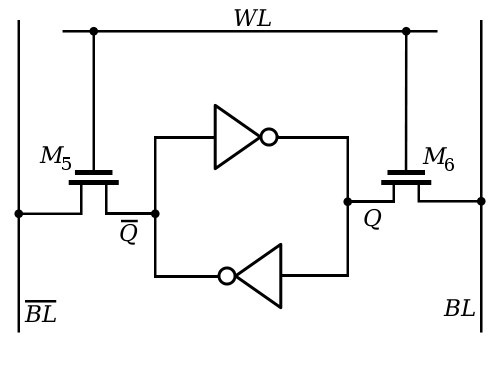
1. Parity, in computer science, is an error checking process based on sameness or equivalence by using the count of 1’s in a bit package transferred to confirm if it is an even or an odd number according to the type of test set beforehand. If it is an even parity test, then the total number of 1’s in a bit package must add up to an even number to show that the data was transferred without any errors. If it is an odd parity test, then the total number of 1’s in a bit package must add up to an odd number in order to represent the successful data transmission. Parity makes information storage more reliable if the storage is made through a transmission. This is because now there is a parity check in effect on the packages, it is possible to detect a package loss or corruption.

References:

* Autocww.colorado.edu. (2000). *Parity (computer science)*. [online] Available at: http://autocww.colorado.edu/~toldy3/E64ContentFiles/ComputersElectronics/Parity.html [Accessed 10 Mar. 2018].



I first drew the truth table that matches the given situation. I found a similarity between XNOR gate’s truth table, so I tried using them. Since there were 4 inputs I connected each 2 of them to 1 XNOR gate and connected their output to another one which will give the final output.

SRAMs’ are almost more than twice the size of DRAMs’. An average DRAM chips which is found in a personal computer can have access times from 50 to 150 nanoseconds where SRAM chips can reach access times down to 10 nanoseconds. Because of this fact, SRAM is more likely to be used for CPU’s cache where for DRAM, it might be a computer’s main memory.

References:

* Anon, (n.d.). [online] Available at: https://www.quora.com/How-does-a-computer-physically-store-digital-data [Accessed 10 Mar. 2018].
* En.wikipedia.org. (2014). *SRAM Cell Inverter Loop.png*. [online] Available at: https://en.wikipedia.org/wiki/File:SRAM\_Cell\_Inverter\_Loop.png [Accessed 10 Mar. 2018].
* Webopedia.com. (n.d.). *What is Access Time? Webopedia Definition*. [online] Available at: https://www.webopedia.com/TERM/A/access\_time.html [Accessed 10 Mar. 2018].

1. A third of 70 years is 23.3 years. 30 frames per second makes 30 million pixels per second. 3 bytes per pixel makes 90 million bytes of data per second. Which then is equal to 6.61311e+16 for 23.3 years. As sound, 176000 \* 23.3 = 1.2932304e+14 bytes of sound data for 23.3 years. A total of 6.6260423e+16 bytes of data for 23.3 years of recording sound and image. Now that is compressed to 10% of the total data which is equal to: 6.6260423e+15.

500 GB of data is 5e+11 bytes of data. If 6.6260423e+15 bytes of data is for 23.3 years, then 5e+11 bytes of data is for 0.00175821394 years.

In the document ‘Road Map for Memories for Life Research’ the topic is taken from another angle. Instead of upgrading our technology to store more data which is enough for a life time, they have taken it as changing the data type, and the way it is stored. Rather than an individual collection of inputs, a collective memory which can be accessed. Therefore, I believe it is a reasonable claim.